As the three-month shortened statutory period for reply is due July 30, 2004, this Response is therefore considered timely filed.

AMENDMENTS

Please change the Attorney Docket No. from "18153.0040" to **--068354.1443--.**

Please note a Change of Mailing Address for prosecution purposes is enclosed herewith.

In the Claims

Applicant respectfully submits that no amendments have been made to the pending claims for the purpose of overcoming any prior art rejections that would restrict the literal scope of the claims or equivalents thereof.

Please cancel claims 2, 6 and 7 without prejudice to file same in a continuation, divisional, continuation-in-part or co-pending application. Please amend the remaining claims as indicated below:

PENDING CLAIMS AND STATUS THEREOF

1. **(currently amended):** A system for overflow and saturation processing, comprising:

an adder, operatively connected to receive first and second operands, and connected to add the operands **to produce a result of the added operands**;

an accumulator, operatively connected to store at least a portion of the **result of the** added operands or at least a portion of a selected one of predetermined constants based on control signals;

guard bits, operatively connected to store the remaining portion of the **result of the** added operands or the remaining portion of the selected one of predetermined constants based on the control signals;

overflow logic operatively connected to the accumulator and to the guard bits so as to indicate overflow of the accumulator; **[[and]]**

saturation logic, operatively connected to the adder, to the guard bits, and connected to provide the control signals based on at least a portion of the **result of the** added operands **and** at least a portion of the guard bits**; and**

logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison.

Claim 2 (canceled)

3. **(currently amended):** The system according to claim **[[2]]** **1**, wherein the saturation logic includes:

a selector operatively connected to selectively provide **a** one of the **result of the** added operands or **a** one of the predetermined constants based on the comparison.

4. **(currently amended):** The system according to claim **[[2]]** **1**, wherein the logic means includes:

means for providing the control signals in accordance with an enable signal and in accordance with the comparison.

5. **(currently amended):** The system according to claim 4, wherein the logic means further includes:

means, responsive to the comparison, for selectively providing the control signals so that the accumulator stores at least a portion of the **result of the** added operands and the guard bits store the remaining portion of the **result of the** added operands, or the accumulator stores at least a portion of a predetermined constant and the guard bits store the remaining portion of the predetermined constant.

Claims 6 and 7 (canceled)